

FIG. 2

DISK ARRAY CONTROLLER

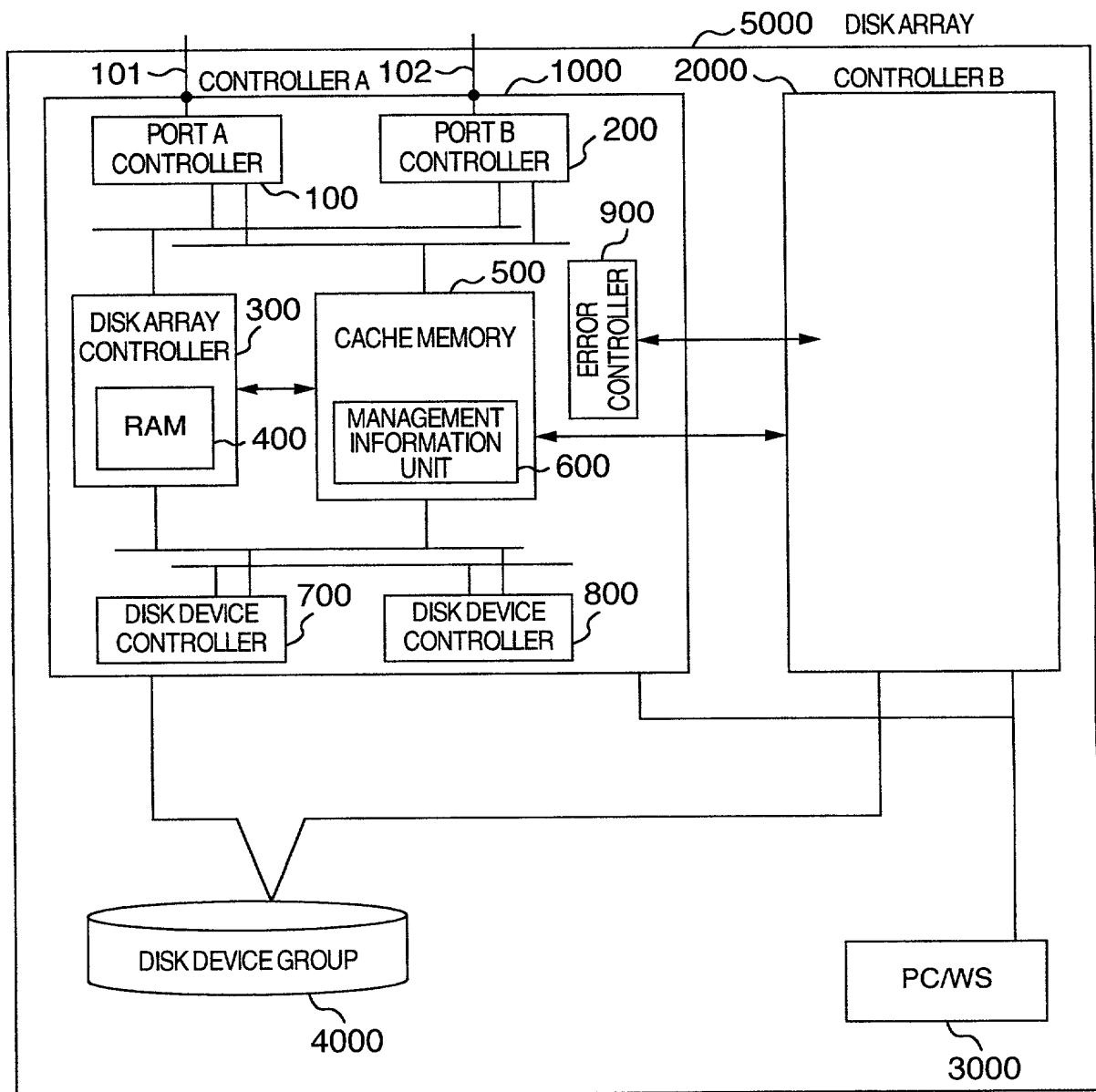


FIG. 4

INTERFACE INFORMATION BETWEEN PORT CONTROLLER
AND DISK CONTROLLER (IN RAM)

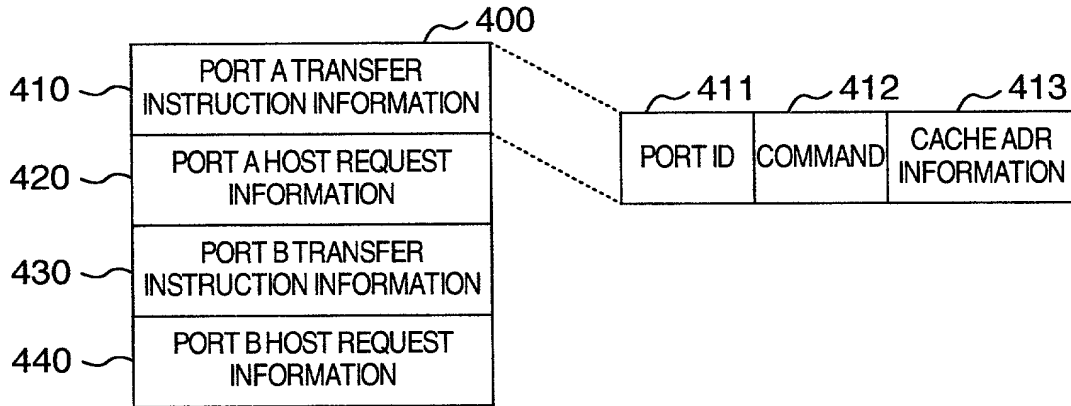


FIG. 5

PORT LOAD INFORMATION (IN RAM)

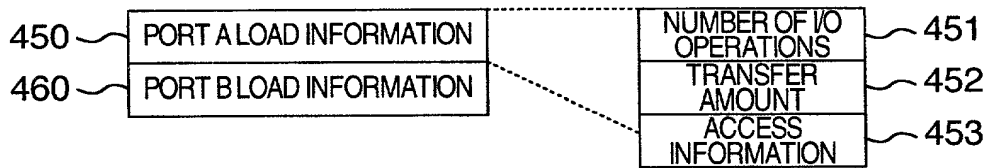


FIG. 6

FIG. 6

CONTROLLER LOAD INFORMATION (IN CACHE)

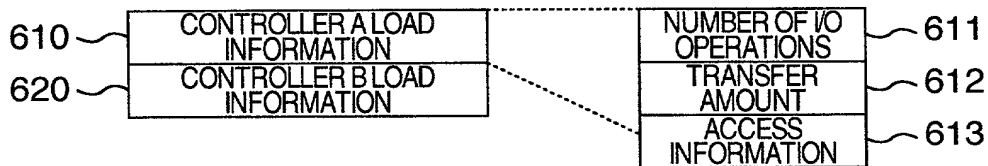


FIG. 7

BACKUP PROGRESS INFORMATION (IN CACHE)

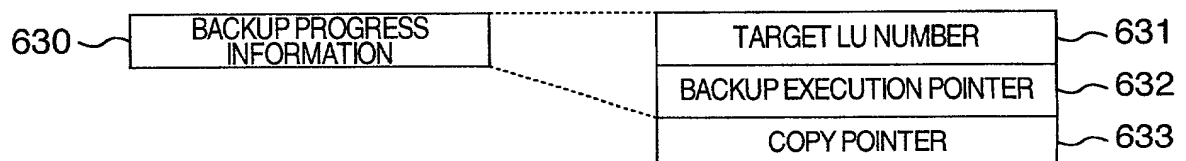


FIG. 8

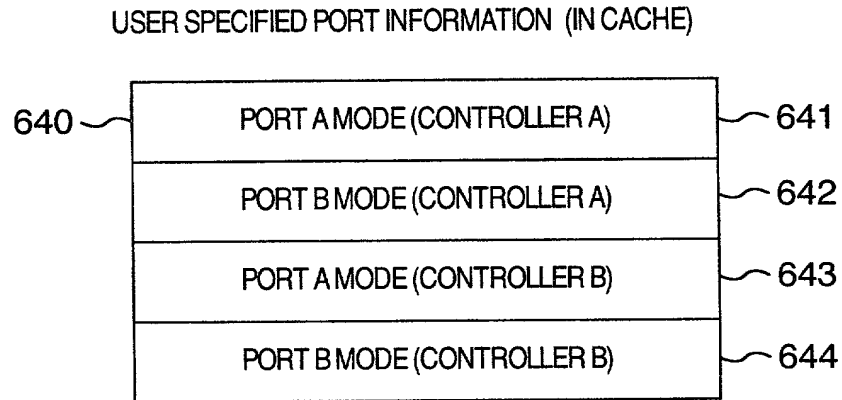


FIG. 9

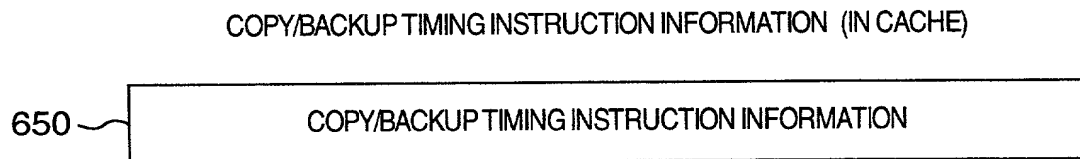


FIG. 10

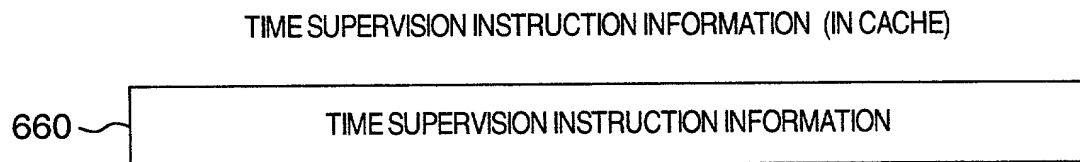


FIG. 11

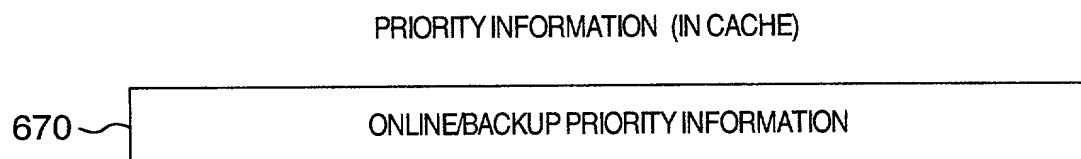


FIG. 12

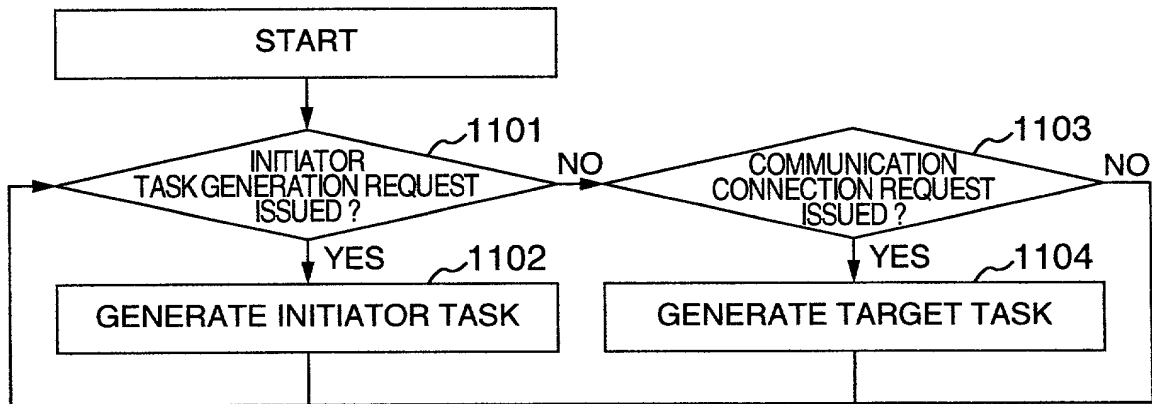


FIG. 13

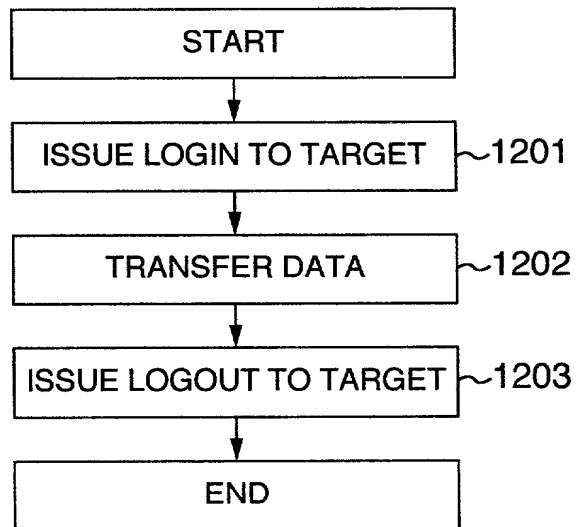


FIG. 14

